DOCKET NO.: P05514 (NATI15-05514) **PATENT**
Customer No.: 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	FRANCISCO JAVIER GUERRERO MERCADO
Serial No.	:	10/619,169
Filed	:	July 14, 2003
For	:	LOW POWER COMPARATOR WITH FAST PROPAGATION DELAY
Group	:	2816
Examiner	:	Tuan Thieu Lam

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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APPELLANT'S REPLY BRIEF

This Reply Brief is submitted on behalf of Appellant for the application identified above.

Please charge any additional necessary fees to Deposit Account No. 50-0208.

ARGUMENT

1. The rejection of claims 7–8 and 15–20 under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement.

a. The limitation "wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock."

In attempting to support the baseless rejection of claims reciting bias current pulses and output sampling triggered by different system clock edges for lack of enablement, the Examiner's Answer states:

> Although, global or system clock signal may be used to coordinate various components in a system, it is still unclear as to how the pulsed bias current is generated from the system clock. This pulsed bias current is being used to bias the input gain stage, one of the inventive features of the present invention, thus providing a gain. The specification briefly mentions the pulse current is produced (page 13, lines 12-14). Since the pulsed current bias is a critical feature of the present invention, it is considered an undue experimentation for one skilled in the art to have to determine how to produce a pulse generator that are capable of generating the pulsed current bias as disclosed in the specification.

Examiner's Answer, pages 7–8. The Examiner's Answer thus seems to suggest that merely producing <u>any</u> pulsed bias current is not enabled by the specification.

Such an assertion is inconsistent with the rejections. Independent claim 1 recites "a pulsed bias current," while dependent claim 7 recites that "the pulsed bias current comprises a pulse at one edge of a system clock." However, claim 1 has not been rejected for lack of enablement, and the feature of a pulsed bias current is asserted in the final rejection to be disclosed by *Heinrich*. Moreover, in disputing the inconsistency of the art rejections with the assertion of lack of

enablement, the Examiner's Answer differentiates the recitation of a simple pulsed bias current in claim 1 from the recitation of a pulses at an edge of the system clock:

> Appellant argues that the application of current Ib of Lim et al. reference and Ic of Heinrich reference to anticipate the "pulse bias current" is contradictory with the rejection of claims 7 and 15 under 35 USC 112, first paragraph is not persuasive. Claims 1-3 and 10-11 (anticipated by Lim); 1-3, 8-11 and 16, 17 (Heinrich) do not call for the pulsed bias current generated in associated with the system clock and the output comparator.

Examiner's Answer, page 8. The Examiner's Answer is thus internally inconsistent, asserting unsupportable arguments simply for the purpose of maintaining a baseless rejection.

Regardless, techniques for producing edge-triggered pulses were well-known to those skilled in the art at the time the application was filed. For example, U.S. Patent No. 6,380,779 entitled EDGE-TRIGGERED, SELF-RESETTING PULSE GENERATOR and issued April 30, 2002 discloses such techniques in conjunction with enabling sense amps within a memory. One skilled in the art would recognize that the circuits disclosed therein can readily be applied to triggering a bias current pulse and/or sampling a comparator output. No undue experimentation is required to produce current pulses, edge-triggered or otherwise.

b. The limitations "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased by a bias current with a different second level value," "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a continuous bias current or in a second mode in which the input gain stage is biased by the pulsed bias current," and "a comparator selectively operating in a first mode in which an input gain stage of the comparator is biased with a pulsed bias current and a second mode in which the input gain stage is biased with a continuous bias current."

In attempting to support the baseless rejection of claims reciting operation in first and second modes for lack of enablement, the Examiner's Answer states:

> [T]he specification fails to describe as to how the mode of operation is selected. Therefore, it would be undue experimentation for one skilled in the art to try to determine how to make a comparator whose bias current is at different level in different modes of operation.

Examiner's Answer, page 8. However, the claims do not recite **selection** of different modes of operation and/or bias current levels, merely that the comparator be capable of operating in different modes. Therefore, "how the mode of operation is selected" is irrelevant to whether a comparator capable of operating in different modes has been enabled.

Regardless, the cited prior art references teach selection of different modes within comparators operating in different modes, including an operating mode and a power saving mode in *Lim* and selection of different bias current levels in *Heinrich*. *Lim*, column 7, lines 36–37; *Heinrich*, Figure 3.

c. The limitation "a current source producing the pulsed or continuous bias current and controlled by the input signal."

In attempting to support the baseless rejection of claims reciting controlling a current source producing either a pulsed or continuous bias current by an input signal, the Examiner's Answer states:

> Regarding the rejection of claim 19 as being non-enablement, appellant points to figure 1 showing the equivalent circuit of figure 1 and concludes that no undue experiment would be required for those skilled in the art to implement the features of claim 19 is not persuasive. Figure 1 shows parameter gm as a pulse controlling the current source (11) for producing a pulsed or continuous bias current. However, the appellant fails to point out as how to implement a circuit in which the **parameter** gm is generated and a current source is controlled by the **parameter** gm is producing the pulsed or continuous bias current. Therefore, it is unclear as to how current source biased by pulsed or continuous bias current and controlled the input signal" is achieved without undue experimentation.

Examiner's Answer, page 9 (emphasis in original). As previously noted, Figure 1 depicts a variable current source I1 within the first (input) gain stage 101 producing bias current ibias and controlled by pulsed (or continuous) transconductance signal gm in a manner similar to Figure 4 (Figure 5 as filed):

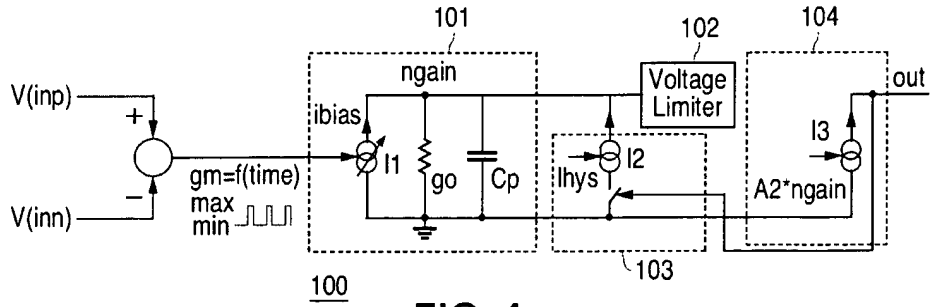

FIG. 1

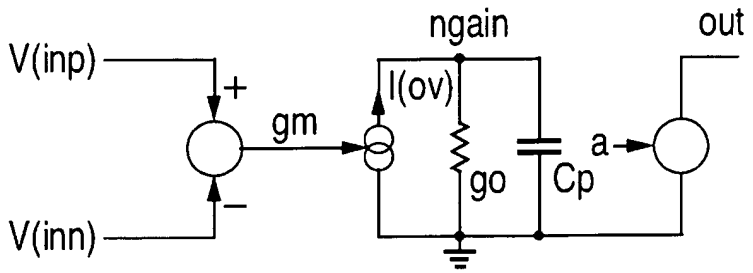

FIG. 5

The specification teaches that the transconductance parameter gm is a function of an input differential pair of CMOS or bipolar junction transistors (now shown in FIGURES 1 or 4):

> [0002] As illustrated in the equivalent circuit diagram depicted in FIGURE 5, integrated circuit comparators typically include: a bias system generating a defined current bias to each transistor; an input differential pair--either complementary metal oxide semiconductor (CMOS) or bipolar junction transistors--that, for a given overdrive voltage V(ov)=(V(inp)-V(inn)) generate a differential current given by I(ov)=gm*V(ov), where gm is the transconductance of the input differential pair at the steady-state operating point V(ov)=0 volts (V); a gain stage node ngain converting the current I(ov) to (in the CMOS case) a voltage gain and having a transition speed depending on the overdrive current I(ov) available, the voltage excursion required between the high and low levels at the ngain node, and the capacitive load at the ngain node, including any Miller capacitance from the comparator's output stage; and a gain stage assuring a given slew rate at the comparator output out.

Specification, ¶ [0002]. Those skilled in the art will understand that when the input transistors are continuously switched on, the transconductance parameter gm will have a continuous value while applying a pulsed control signal to the gates of the input transistors will produce a pulsed transconductance parameter gm.

In addition, the Examiner's Answer cites *Sedra et al* as teaching that the transconductance parameter gm may be produced across the collector and emitter of a bipolar transistor:

> Sedra et al. clearly proves that transconductance parameter is directly proportional to the collect current of a bipolar transistor. Thus, the collector current along the collect-emitter path of the input transistors Q8 and Q9 is the input signal (gm).

Examiner's Answer, pages 9–10. Once again, the Examiner's Answer makes an unsupportable assertion – that undue experimentation would be required for those skilled in the art to "to implement a circuit in which the parameter gm is generated" – contrary to the asserted prior art rejections.

2. The rejection of claims 1–3 and 10–11 under 35 U.S.C. § 102(e) as being anticipated by *Lim*.

The Examiner's Answer asserts that, contrary to the specification, the term "pulsed" and the the claim limitation "pulsed bias current" does not require pulsing of the bias current in accordance with the system clock, but is instead satisfied by the continuous bias current of *Lim*, which may selectively be turned on and off. However, the final rejection and the Examiner's Answer offer absolutely no evidentiary support for such an interpretation of the term "pulsed." No use of the term "pulsed" in *Lim* to describe the continuous bias current of Figure 5c (as opposed to the trigger signal and the output signal of the comparator disclosed in *Lim*) has ever been identified, and no dictionary or technical definition has been cited supporting such an interpretation. Accordingly, the suggested interpretation of the term "pulsed" and the claim limitation "pulsed bias current" are completely arbitrary and capricious.

3. The rejection of claims 1–3, 8–11 and 16–17 under 35 U.S.C. § 102(e) as being anticipated by *Heinrich*.

The Examiner's Answer asserts that, contrary to the specification, the term "pulsed" and the the claim limitation "pulsed bias current" does not require pulsing of the bias current in accordance with the system clock, but is instead satisfied by the varying-level but continuous bias current of *Heinrich* between the higher level and the lower level. However, the final rejection and the Examiner's Answer offer absolutely no evidentiary support for such an interpretation of the term "pulsed." The term "pulsed" does not appear anywhere within *Heinrich*, and in particular is not employed to describe the varying continuous bias current Ic1 of Figure 3. No dictionary or technical definition has been cited supporting the interpretation suggested in the final rejection and Examiner's Answer. Accordingly, the suggested interpretation of the term "pulsed" and the claim limitation "pulsed bias current" are completely arbitrary and capricious.

CONCLUSION

The subject matter of claims 7–8 and 15–20 is enabled by the specification as filed. Therefore, the rejection of claims 7–8 and 15–20 under 35 U.S.C. § 112, first paragraph is improper. The cited references fail to disclose every limitation of the claimed invention. Therefore, the rejections of claims 1–3, 8–11 and 16–17 under 35 U.S.C. § 102 are improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting pending claims 1–3, 7–11 and 15–20 in this application.

Respectfully submitted,

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Date: Aug 29, 2006

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